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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,748	12/29/2003	Kiyoshi Kase	SC13037TC	6133
23125	7590	03/02/2005	EXAMINER TAN, VIBOL	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			ART UNIT 2819	PAPER NUMBER

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/747,748	Applicant(s) KASE ET AL.	
	Examiner Vibol Tan	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2003.  
2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-3, 6, 7, 11-16, 18-30, 33-39 and 41-43 is/are rejected.  
7) ☒ Claim(s) 4, 5, 8-10, 17, 31, 32 and 40 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/29/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the difference in thicknesses of the gate dielectric of the first and the second transistors in claim 27 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

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2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 13-16, 18 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 13-16, it is not clearly understood of the connection arrangements for each of the claims. Please direct to the drawings the locations of the non inverting output and the inverting output.

In claims 18 and 33, if the first configuration includes an additional transistor, this would mean the first threshold voltage is greater than the second threshold voltage which contradicts the recitation in claims 1 and 29, respectively.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6, 7, 22-26, 28-30, 34-37, 39 and 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Rosen (U. S. PAT. 6,822,479).

In claim 1, Rosen teaches all claimed features in Fig. 2, a level shifter comprising: a first inverter (230) having a first threshold voltage (a first required voltage

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to turn on transistor 236 of inverter 230); and a second inverter (220) having a second threshold voltage (a second required voltage to turn on transistor 226 of invert 220), the second threshold voltage being greater than the first threshold voltage (due to additional transistor 227) by at least a predetermined amount (a difference between the first required voltage and the second required voltage), wherein the first inverter and the second inverter are cross-coupled (as shown in Fig. 2).

In claim 2, Rosen further teaches the level shifter of claim 1 wherein: the first inverter (230) has a first configuration of transistors (234, 236) and the second inverter has a second configuration of transistors (224-227); the second configuration includes an additional transistor (227) not found in the first configuration.

In claim 3, Rosen further teaches the level shifter of claim 2, wherein the additional transistor (227) is an N-channel transistor.

In claim 6, Rosen further teaches the level shifter of claim 1 wherein: the first inverter comprises a first P-channel transistor (234) connected in series to a first N-channel transistor (236); the second inverter comprises a second P-channel transistor (224) connected in series to a second N-channel transistor (226), wherein a third N-channel transistor (227) is connected in series with the second N-channel transistor (226).

In claim 7, Rosen further teaches the level shifter of claim 1 wherein: the first inverter (230) consists essentially of two transistors connected in series (234, 236); the second inverter (220) consists essentially of three transistors connected in series (224, 227, 226).

In claim 22, Rosen further teaches the level shifter of claim 1 wherein: an output connected to one of an output of the first inverter and an output of the second inverter (output of 220); drive circuitry (250) connected to the output.

In claim 23, Rosen further teaches an integrated circuit (col. 3, line 16) including the level shifter of claim 1.

In claim 24, Rosen further teaches the integrated circuit of claim 23 further comprising: a first circuit (206) coupled to an input (gate of 208) of the level shifter, the first circuit being powered from a first voltage source (1.5V; col. 1, line 18); a second circuit (250) coupled to an output (output of 220) of the level shifter, the second circuit being powered from a second voltage source (2.5V; col. 1, line 21) wherein the second voltage source powers up before the first voltage source (col. 4, lines 14-17); wherein an output of the level shifter is at a known voltage state prior to a powering up of the first voltage source (col. 4, lines 14-17); wherein the output of the level shifter (output of the level shifter is an output of 220) is connected to one of an output of the first inverter or an output of the second inverter.

In claim 25, Rosen further teaches the level shifter of claim 1 wherein: the first inverter (230) includes an input and an output (see 230 in Fig. 2); the second inverter (220) includes an input and an output (see 220 in Fig. 2); the output of the first inverter is connected to the input of the second inverter and the output of the second inverter is connected to the input of the first inverter (as shown in Fig. 2).

In claim 26, Rosen further teaches the level shifter of claim 1 wherein: the first inverter (230) has a first transistor (234) configuration with a first ratio of strength

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(strength of 234 over strength of 236) of a first channel type transistor to strength of a second channel type transistor (236); the second inverter (220) has a second transistor configuration with a second ratio of strength (strength of 224 over strength of 2227) of a first channel type transistor (224) to strength of a second channel type transistor (227); the first ratio is different than the second ratio by at least a predetermined amount (due to the additional transistor pair 225, 227).

Claims 27 and 28, each corresponds to detailed circuitry already discussed similarly with regard to claim 26.

Claims 29 and 30 correspond to detailed circuitry already discussed similarly with regard to claims 1 and 2.

Claims 34-37, 39 and 43 correspond to detailed circuitry already discussed similarly with regard to claims 1-3, 6 and 43.

In claim 41, Rosen further teaches the level shifter of claim 34 further comprising: an output (a terminal coupling to an output of 230), the output connected to an output of the first inverter (230).

In claim 42, Rosen further teaches the level shifter of claim 34 further comprising: an output (a terminal coupling to an output of 220), the output connected to an output of the second inverter (220).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 11 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosen in view of applicant's admitted prior art of Fig. 1.

In claims 11 and 12, Rosen further teaches the level shifter of claim 1; with the exception of teaching wherein: the first inverter includes a first transistor having a first current terminal coupled to an output of a voltage source and a second current terminal coupled to an output of the first inverter (; the second inverter includes a second transistor having a first current terminal coupled to the output of the voltage source and a second current terminal coupled to an output of the second inverter; during power up of the voltage source, an output of the first inverter is pulled to a low voltage state when a voltage of the output of the second inverter exceeds the threshold voltage of the first inverter. However, applicant's admitted prior art of Fig. 1 teaches the first inverter (104) includes a first transistor (113) having a first current terminal coupled to an output of a voltage source (ground) and a second current terminal coupled to an output of the first inverter (104); the second inverter (106) includes a second transistor (115) having a first current terminal coupled to the output of the voltage source (ground) and a second current terminal coupled to an output (114) of the second inverter; during power up of the voltage source, an output of the first inverter is pulled to a low voltage state (to ground because 107 conducting) when a voltage of the output of the second inverter exceeds the threshold voltage of the first inverter.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Rosen with the teachings of



applicant's admitted prior art of Fig. 1 to prevent the output of the activation signal until the core voltage is supplied to the integrated circuit to limit any damage of contention.

In claim 38, Rosen teaches all claimed features of the level shifter of claim 34; with the exception of teaching wherein the additional transistor is a, P-channel transistor. It would have been obvious to one ordinary skill in the art at the time the invention was made to switch an N-channel transistor with a P-channel transistor since it was known that switching between the transistor types involves only routine skill in the art.

8. Claims 4, 5, 8-10, 17, 31, 32 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**VIBOL TAN**  
**PRIMARY EXAMINER**